

IN THE CLAIMS

Claims 1-25 were in the original application.

Please cancel claims 1, 8, and 15.

Please amend claims 2-7, 9-14, and 16-25 as follows:

Please amend claims 2-7, 9-14, and 16-24 as follows:

A2 1 2 (Amended). The [method] integrated circuit of Claim [1] 22,
2 wherein said deposition step (c.) is plasma-enhanced.

1 3 (Amended). The [method] integrated circuit of Claim [1] 22,
2 wherein said deposition step (c.) uses TEOS as a source gas.

1 4 (Amended). The [method] integrated circuit of Claim [1] 22,
2 comprising the additional step of applying a passivating
3 dielectric, under vacuum conditions, after said step (a.) and
before said deposition step (b.).

1 5 (Amended). The [method] integrated circuit of Claim [1] 22,
2 wherein said deposition step (b.) applies said spin-on glass with
3 a thickness in the range of 1000-5000Å inclusive.

1 6 (Amended). The [method] integrated circuit of Claim [1] 22,
2 wherein said deposition step (d.) applies said spin-on glass with
3 a thickness in the range of 1000-5000Å inclusive.

1 7 (Amended). The [method] integrated circuit of Claim [1] 22,
2 wherein said interlevel dielectric is a doped silicate glass.

A3 1 9 (Amended). The [method] integrated circuit of Claim [8] 23,
2 wherein said deposition step (c.) is plasma-enhanced.

1 10 (Amended). The [method] integrated circuit of Claim [8] 23,
2 wherein said deposition step (c.) uses TEOS as a source gas.

1 11 (Amended). The [method] integrated circuit of Claim [8] 23,
2 comprising the additional step of applying a passivating

3 dielectric, under vacuum conditions, after said step (a.) and
4 before said deposition step (b.).

1 12 (Amended). The [method] integrated circuit of Claim [8] 23,
2 wherein said deposition step (b.) applies said spin-on glass with
3 a thickness in the range of 1000-5000Å inclusive.

1 13 (Amended). The [method] integrated circuit of Claim [8] 23,
2 wherein said deposition step (d.) applies said spin-on glass with
3 a thickness in the range of 1000-5000Å inclusive.

1 14 (Amended). The [method] integrated circuit of Claim [8] 23,
2 wherein said interlevel dielectric is a doped silicate glass.

16 (Amended). The [method] integrated circuit of Claim [15] ²⁴,
wherein said deposition step (c.) is plasma-enhanced.

17 (Amended). The [method] integrated circuit of Claim [15] ¹⁵ 24,
wherein said deposition step (c.) uses TEOS as a source gas.

18 (Amended). The [method] integrated circuit of Claim [15] 24,
comprising the additional step of applying a passivating
dielectric, under vacuum conditions, after said step (a.) and
before said deposition step (b.).

1 19 (Amended). The [method] integrated circuit of Claim [15] 24,
2 wherein said deposition step (b.) applies said spin-on glass with
3 a thickness in the range of 1000-5000Å inclusive.

1 20 (Amended). The [method] integrated circuit of Claim [15] ¹⁷
2 wherein said interlevel dielectric is a doped silicate glass.

1 21 (Amended). The [method] integrated circuit of Claim [15] 24,
2 wherein said deposition step (d.) applies said spin-on glass with
3 a thickness in the range of 1000-5000Å inclusive.

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1 22 (Amended). An integrated circuit manufactured by the method
2 [of claim 1.] comprising the acts of:
3 (a.) providing a partially fabricated integrated circuit
4 structure;
5 (b.) applying and curing spin-on glass, to form a first
6 dielectric layer;
7 (c.) depositing dielectric material, to form a second dielectric
8 layer over said first dielectric layer;
9 (d.) applying and curing spin-on glass, to form a third
10 dielectric layer, to produce a stack including said third
11 dielectric layer over said first and second dielectric layers;
12 (e.) performing a global etchback to substantially remove
13 portions of said dielectric stack from high points of said
14 partially fabricated structure, wherein at least a portion of
15 said third dielectric layer remains after said global etchback;
16 (f.) deposition of an interlevel dielectric at least over said
17 remaining third dielectric layer;
18 (g.) etching holes in said interlevel dielectric in predetermined
19 locations; and
20 (h.) depositing and patterning a metallization layer to form a
21 desired pattern of connections, including connections through
22 said holes.

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1 23 (Amended). An integrated circuit manufactured by the method
2 [of claim 8.] comprising the acts of:
3 (a.) providing a partially fabricated integrated circuit
4 structure;
5 (b.) applying and curing spin-on glass, to form a first
6 dielectric layer;
7 (c.) depositing silicon dioxide, to form a second dielectric
8 layer over said first dielectric layer;
9 (d.) applying and curing spin-on glass, to form a third
10 dielectric layer to produce a dielectric stack including said
11 third dielectric layer over said first and second layers;
12 (e.) performing a global etchback to substantially remove said
13 dielectric stack from high points of said partially fabricated

14 structure, wherein at least a portion of said spin-on glass of
15 said third dielectric layer remains after said global etchback;
16 (f.) deposition of an interlevel dielectric at least over said
17 remaining spin-on glass of said third dielectric layer;
18 (g.) etching holes in said interlevel dielectric in predetermined
19 locations; and
20 (h.) depositing and patterning a metallization layer to form a
21 desired pattern of connections, including connections through
22 said holes.

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1 24 (Amended). An integrated circuit manufactured by the method
2 [of claim 15.] comprising the acts of:
3 (a.) providing a partially fabricated integrated circuit
4 structure;
5 (b.) applying and curing spin-on glass, to form a first
6 dielectric layer;
7 (c.) depositing dielectric material, to form a second dielectric
8 layer over said first dielectric layer, said second dielectric
9 layer having a thickness equal to or less than said first
10 dielectric layer;
11 (d.) applying and curing spin-on glass, to form a third
12 dielectric layer to produce a dielectric stack including said
13 third dielectric layer over said first and second dielectric
14 layers, said third dielectric layer having a thickness equal to
15 or greater than said second layer;
16 (e.) performing a global etchback to substantially remove said
17 dielectric stack from high points of said partially fabricated
18 structure, wherein at least a portion of said third dielectric
19 layer remains after said global etchback;
20 (f.) deposition of an interlevel dielectric at least over said
21 remaining second dielectric layer;
22 (g.) etching holes in said interlevel dielectric in predetermined
23 locations; and
24 (h.) depositing and patterning a metallization layer to form a
25 desired pattern of connections, including connections through
26 said holes.